semiconductor layers because of the use of the word "like." Applicants have amended each of the claims so that they now recite -- semiconductor islands -- . It is respectfully submitted that this overcomes the Examiner's objection to the claims. Accordingly, it is requested that this rejection now be withdrawn.

Claim Rejections - 35 USC §103

The Examiner also rejects Claims 29, 31 and 33 under 35 U.S.C. §103(a) as being unpatentable over Ohtani et al. in view of Fukuda et al. This rejection is respectfully traversed.

Applicants have amended independent Claim 29 herein to clarify the step of forming n type impurity regions having a second concentration to now recite:

> "forming n type impurity regions having a second concentration, for forming source regions or drain regions outside said LDD regions by introducing an n-type impurity thereinto while covering at least said LDD regions of said n channel type TFT of said driving circuit and said pixel TFT with resist masks, respectively;"

This step is shown, for example, on page 22 of the specification and in Fig. 2(c).

Neither of the cited references disclose or suggest such a step. As the Examiner acknowledges, Ohtani does not disclose the step of forming n type impurity regions having a second concentration, as recited in Claim 29 and therefore cites Fukuda, Figs. 7A-7H. In these figures, however, Fukuda does not disclose or suggest forming n type impurity regions having a second concentration, for forming source regions or drain regions outside the LDD regions by introducing an n-type impurity thereinto while covering at least the LDD regions of the n channel type TFT of said driving circuit and said pixel TFT with resist masks, respectively, as required in amended claim 29.

Therefore, since the method in independent Claim 29, and those claims dependent thereon, is not disclosed or suggested by the cited references, these claims are patentable thereover. Accordingly, it is requested that this rejection now be withdrawn.

The Examiner also have the following further rejections of the dependent claims: Claim 30 under 35 U.S.C. §103(a) as being unpatentable over Ohtani et al. in view of Fukuda et al. and further in view of Zhang et al. and Claim 32 under 35 U.S.C. §103(a) as being unpatentable over Ohtani et al. in view of Fukuda et al. and further in view of Yamamoto et al. Each of these dependent claims are patentable over the cited references for at least the reasons discussed above for the independent claims. Accordingly, it is requested that these rejections now be withdrawn.

Therefore, it is respectfully submitted that all of the rejections under §103 have been overcome.

New Claims

Applicants are also adding new dependent Claims 53-63 herewith. It is believed that these claims should be allowable over the art for at least the reasons discussed above. It is not believed that a fee is due for these claims. If a fee should be due, please charge our deposit account 50/1039.

Acknowledgment of IDS

Applicants also request acknowledgment and consideration of the IDS and 1449 filed on October 26, 2001 in this application.

Conclusion

For the above stated reasons, the present application is now in a condition for allowance and should be allowed.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

Date: December 20, 2002

Mark J. Murphy
Registration No. 34,225

COOK, ALEX, McFARRON, MANZO,
CUMMINGS & MEHLER, LTD.
200 West Adams Street; Suite 2850
Chicago, Illinois 60606
(312) 236-8500

Marked-up copy of the claims as amended:

IN THE CLAIMS:

Please amend the claims as follows:

29 (Amended). A method of fabricating a semiconductor device having, on the same substrate, a pixel TFT disposed in a pixel unit and a driving circuit including a p channel type TFT and an n channel type TFT and disposed round said pixel unit, said method comprising [the steps of]:

forming an underlying film over said substrate;

forming a plurality of [island-like] semiconductor [layers] islands over said underlying film;

forming n type impurity regions having a first concentration, for forming LDD regions of said n channel type TFT of said driving circuit and said pixel TFT in selected regions of said [island-like] semiconductor [layers] islands;

forming n type impurity regions having a second concentration, for forming source regions or drain regions outside said [n type impurity regions having the first concentration] LDD regions by introducing an n-type impurity thereinto while covering at least said LDD regions of said n channel type TFT of said driving circuit and said pixel TFT with resist masks, respectively;

forming a p type impurity region having a third concentration, for forming a source region or a drain region of said p channel type TFT of said driving circuit in a selected region of said [island-like] semiconductor [layer] islands;

forming a protective insulation film [formed of] comprising an inorganic insulating material [above] over said n channel type TFT of said driving circuit, said pixel TFT and said p channel type TFT;

forming an inter-layer insulation film [formed of] comprising an organic insulating material in close contact with said protective insulation film; and

forming [on] over said inter-layer insulating film a pixel electrode having a light reflecting surface and connected to said pixel TFT.

30 (Amended). A method according to claim 29, wherein, as for said p channel type TFT of said driving circuit, the step of forming a p type impurity region having a third concentration, for forming a source region or a drain region of said p channel type TFT is conducted in a selected region of said [island-like] semiconductor [layers] islands after said step of forming said protective insulation film [formed of] comprising an inorganic insulating material, [on] over the gate electrode of said p channel type TFT, and an offset region is formed between the channel formation region of said p channel type TFT and said p type impurity region having the third concentration, for forming the source region or the drain region.

Please add the following new claims:

53 (New). A method according to claim 31 wherein said low resistance conductive material comprises a material selected from the group consisting of Al and Cu.

54 (New). A method according to claim 29 wherein said protective insulation film comprises a material selected from the group consisting of silicon oxide, silicon oxide nitride and silicon nitride.

55 (New). A method according to claim 29 wherein said protective insulation film has a thickness of 100 to 200 nm.

56 (New). A method according to claim 29 wherein said inter-layer insulation film has a mean thickness of 1.0 to 2.0 μm.

57 (New). A method according to claim 29 wherein said inter-layer insulation film comprises a material selected from the group consisting of polyimide, acryl, polyamide, polyimidamide and benzocyclobutene.

58 (New). A method according to claim 29 wherein said pixel electrode comprises a Ti film and an Al film.

59 (New). A method according to claim 29 wherein said p channel type TFT has a single drain structure.

60 (New). A method according to claim 29 wherein said LDD regions of said n channel type TFT of said driving circuit have a length of 1.0 to 4.0 μm.

61 (New). A method according to claim 29 wherein said LDD regions of said n channel type TFT of said pixel TFT have a length of 0.5 to 4.0 μm.

62 (New). A method according to claim 29 wherein said semiconductor islands have a thickness of 25 to 80 μm.

63 (New). A method according to claim 29 wherein said driving circuit comprises a circuit selected from the group consisting of a shift register circuit, a level shifter circuit, a buffer circuit and sampling circuit.